High Speed Counter LFSR State Extension with Clock Gating Technique

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ABSTRACT
In this study, a fast counter design is coupled with anunusual LFSR state extension. Using the proposed state extension, a redesigned m-bit LFSR clock with 62 million 1Ð states can manage 2 million states without decreasing the counting pace. By consistently exchanging just the low-order bits, the proposed counter is able to achieve a high recounting rate while reducing the hardware complexity required to transition straight into a binary phase from an LFSR format. Comprising it are two sub-counters. The sub-counter at the lowestorder is implemented using the proposed LFSR counter, whereas the high-order sub-counter is created using the traditional synchronous binary counter. Since the high-order sub-counter has a hugefan-out, the used counter also takes it into consideration when calculating the speed loss. The proposed 65 nm CMOS counter operates at 2.08 GHz and is constructed using standard pixels; its calling rate is virtually size independent.

Keywords: LFSR, D Flipflop, CMOS, Phase shifting, FMCW, FFD

1.INTRODUCTION

There have been a lot of recent developments that have increased the need for quick counters capable of handling wide bit widths. This class of functionalities includes things liketime-to-digital converters, analog-to-digital converters, phase-locked loops, and frequencysynthesizers. Places. To achieve a high counting rate with a standard binary counter, the counter sizemust be very small due to the intrinsicincompatibility between the two. Additionally, most asynchronous binary counters that combine a state register with an adder do not achieve an ongoing clock rate that is independent from because theadder's latency is proportional to the counter's size. You can make a counter that is synchronous that operates at constant time using a state generator when you don't need the binary state right away. A number of state generators are available, including the LFSR (linear feedback shift register). Using the current state to direct the future state, this concept contains a feedback relationship. Using merely two Special D flip-flops-AND (XOR) gates, the LFSR may be implemented to generate a synchronous counter that operates at constant time and with fast speed. and its delay is almost size independent. when citing references happens. Mentioned in the feedback connection differentiates between two types of LFSR. Operating velocity of the a many-to LFSR lowers according to rising input bit counts, much like a binary counter [14]. The ratio LFSR is a variant that use a single F/F result to feed backward into several successive F/Fs. The first kind of LFSR is called a many-to-one LFSR, and itemploys several F/Fs to produce a single feedback value. The speed disparity, however, has been ignored in a number of earlier studies that relied onmany-to-one LFSRs as its foundational counter.

A digital CMOS vision sensor uses a counter to transform the analogue dots into digital ones, as shown. The many-to-one LFSR counter that is built- in makes this conversion a breeze. Furthermore, pseudo-random sequences may be generated using a many-to-one LFSR counter if the physically unclonable function is based on ring oscillators. In addition, a time-of-flight camera system with a multiple-step LFSR counter was developed using amany-to-one LFSR, as mentioned in references with. Before employing the LFSR for the count, it is important to carefully evaluate one potential downside. To increase the quantity of levels to 2m and convert an LFSR condition to a binary state, extra circuits are required, as an m-bit LFSR can only be linked to a maximum number of (2m 1) states. If the counting rate needs to be constant, thestate elongation and LFSR, which must happen at the same time. By integrating iterate and indirect look-up device (LUT) techniques, the authors of provide a time-memory tradeoff. The time-memory tradeoff does not account for state extension hence it is not possible to transform an LFSR state to a binstate. Additionally, the LUT size grows exponentially with the counter size. While a multistage LFSR clock was described, the invention is accompanied by a state extension that drastically decreases counting speed and a direct correlation between the size of the counter and the level ofcomplexity if the decoding circuitry. Associatedwith a new state implication, this article presents a high-speed counter. Two subsections make up the proposed counter. counters: one that is binary and the other that is LFSR, maintains a nearly constant latency over a variety of counter sizes. With the proposed counter's state detecting circuit, an m-bit LFSR counter can go from 2m 1 to 2m states without slowing down the counting pace. We designa counter prototype using conventional cells and putit through its paces in 65 nm CMOS semiconductors. After that, we check it against previous counts. The counting pace of the prototypecounter is higher than that of its forerunners.

2.RELATED WORK

"A 0.045- to 2.5-GHz frequency synthesizer with TDC-based AFC and phase switching multi- modulus divider"

Our research presents a frequency synthesizer (FS) with a broad working frequency range of 0.045 to 2.5 GHz. It employs a phase-switching multi- modulus divide (MMD) and an AFC technique that depends on time-to-digital converter (TDCs) to reduce quantization noise. While the counter-based AFC technique needs a large number of reference cycles to get the immediate VCO frequency, the suggested TDC-based method only requires two cycles. The quantization of the noise produced by the sigma-delta multiplexed (SDM) within an MMD might be mitigated via the phase shifting (PS) approach by reducing the loop split step from 2 to 0.5. A TSMC 180nm RF Semiconductor design and model were used to create the FS. The AFC time computations, using a 48 MHz reference signal, reveal an average time of 1.4 µs, and the amount of quantization noise is 12 dB lower compared to the typical MMD structure.

"High speed digital CMOS divide-by-nfrequency divider,":

Our solution is based on very simple digital CMOS circuitry and is scalable up to N frequencies. A combination of a pipelined design and a novel parallel counter allows the divider to operate at high speeds. All changes to state values are triggered concurrently by the parallel counter, which uses the internal pipeline structure and a status look-ahead feature to prevent rippling effects. Because subtractor circuitry "swallows" additional cycles, pipeline delays aren't an option. In addition, the modular design of our frequency divider makes it easy to extend it to suit very broad divisions. Because the fan-in and fan-out both width independent, the structure is appealing for frequent VLSI executions and ongoing technological improvement. We put our proposed divider into action by scanning a 0.15-µm TSMC digital cell bank, which provides 252 unique frequency divisions. Operating at 2 GHz, this 8-bit logic chip consumes 15.47 mW of power, has a dimension of 112,848 µm2 (900 chips), and can reach a maximum working frequency of 2 GHz.

"A 12-GHz calibration-free all-digital PLL for FMCW signal generation with 78 MHz/ms chirp slope and high chirp linearity,"

This work presents a novel approach to high-linear FMCW signal production using all-digital phase- locked loops (ADPLL). By using the two-point modulated (TPM) method, a rapid chirp slope may be attained. The digitally-controlled oscillating (DCO) technique, with its broad loop bandwidth, effectively prevents ramp linearity distortion. A digital phase interpolator (DPI) based calibration- free retiming fractions division of tones (FFD) approach is suggested to handle quantization noise and the bandwidth constraint of the loop. In order to achieve high-linear phase interpolation, the retiming FFD system makes use of a parasite-insensitive DPI. In order to further decrease quantization noise, a vernier time-to-digital converter (TDC) with a temporal resolution of 2.3 ps and an exceptionally high bandwidth digital-to-analog converter (DCO) with a least substantial bit (LSB) of 9.8 kHz/bit are also used. Power consumption is 33.8 mW, and the integrated area is 0.32 mm 2 for the 40-nm CMOS ADPLL prototype. The data reveals that a chirp inclination of up to 78 MHz is attained, along resulting in a root-mean-square (RMS) pitched error of up to 167 kHz. One millisecond of sweeping the frequency range from 300 MHz to 100 MHz results in an RMS frequency error of 5.6 kHz at its lowest. The phase noise produced by the 12.15 GHz pulse has an offset of 1 MHz, or -113.6 dB/Hz.

"A CMOS pixel with embedded ADC, digital CDS and gain correction capability for massively parallel imaging array,"

The research suggests a complementary metal-oxide semiconductor (CMOS) pixel for photography arrays that can simultaneously correct for light responsive non-uniformity (PRNU) and black signal variation (DSNU), enabling very concurrent image acquisition. Each pixel in our system is a fully functioning block, thanks to its integrated light sensor and ADC with correlated double sampling (CDS). It is implemented using the standard 0.18 µm CMOS technology. The size of one pixel having a 9-bit accuracy is 21 µm × 21 µm. Data collected using a 128 × 128 image matrix confirms that the proposed approach is functional. When using CDS, light FPN decreases to 14 LSB (3.7%) to 7 LSB (1.8%), while
darkness FPN decreases from 12 LSB (3% to 0.8 LSB, or 0.2%). To do this, PRNU was compensated using massively parallel creative digital multiplication, which results in a light FPN of around 1 LSB, has a high resolution (1/511), and does not interfere with simultaneously processed CDS. It may also be implemented within a small pixel area.

3. PROPOSED SYSYTEM

PREVIOUS COUNTERS:

Here you will find information on the classic binary counter, the pre-scaled counter, and the LFSR. Following that, a brief summary of the literature on the LFSR clock is provided. Trader in Binary Options Figure 1 shows the classic synchronous binary counter, the component that generates a binary sequence. The counter consists An innovative method for producing high-linear FMCW signals utilising ADPLL is introduced in this study. The two-point manipulated (TPM) technique allows for the quick chirp slope to be achieved. The digitally-controlled oscillatory (DCO) method successfully eliminates ramp linearity distortion thanks to its broad

bandwidth for loops. Our solution to quantization noise and the bandwidth constraint of the loop is a calibration-free retiming fragmentation divisions and tones (FFD) approach that uses a digital phase interpolator (DPI). The retiming FFD technology accomplishes high-linear phase interpolation by use of a parasite-insensitive DPI. The vernier-type time-to-digital converters (TDCs) and the exceptionally high-width digital-to-analog convert (DCO) both have LSBs of 9.8 kHz/bit. resolution for time of 2.3 ps are also used to furtherreduce quantization noise. The 40-nm CMOS ADPLL concept has an integrated area of 0.32 mm 2 and a power consumption of 33.8 mW. The data shows that a chirp angle of up to 78 MHz is achieved, which leads to a root-mean-square (RMS)pitch error of up to 167 kHz. The RMS frequency error drops to 5.6 kHz at the lowest level after one millisecond of checking the frequency spans 300 MHz to 100 MHz. A 1 MHz offset, or -113.6 dBc/Hz, characterizes the phase noise generated by the 12.15 GHz pulse. All of the F/Fs have EN ports and CLK, except for the first one, which has an XOR gate connected to the CNT signal. A ripple carry chain, a set of AND gates, is used to execute the binary sequence's condition that all low bits be 1. Since the chain's outputs are only valid if all the smaller results havestabilised, it generates a critical pathway that limits the counting speed. You can't utilise the chain whena large counter is needed since its propagation time depends on the dimensions of the counter.

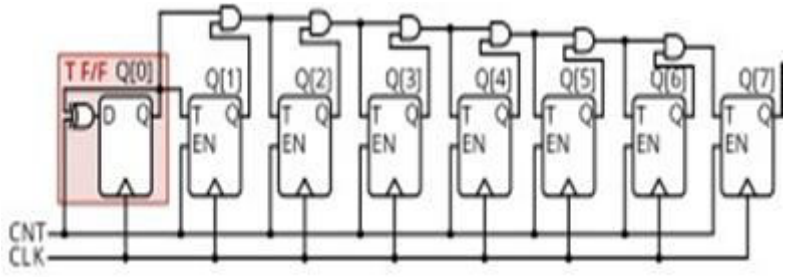

Fig: 3.1 Conventional 8-bit synchronous binary counter

Pre-Scaled Counter

The In Figure 2, N-bit pre-scaled sensors are shownto provide a size-independent uninterrupted counting rate, as proposed in [19]. Since there are m pieces and ðNm bits in the counter, it is split in half since m is considerably smaller than N. Due to the high-order sub-counter's need for a long clock period, the ith bit within the counting signal changes position every 2i clock cycles [7], [20]. Because of [19], the high-order sub-counter may run slowly, even though the low-order sub-counter requires just
6 bits or less. After in 2m-state low-order sub- counter finishes counting, the high-order sub- counter is activated using a 2m-bit linear ring counter, as seen in the top-right viewpoint of Figure
2. Each clock cycle begins with a one-position rightward shift of the countdown ring and a one- position initialization of the F/F value on the opposing side of the more tightly spaced rings clock.You can't utilize the pre-scaled counters until two big concerns are resolved. Just a friendly reminder that the measuring area for each straighter ring countis directly related to 2m, therefore the number of F/Fs required grows exponentially with m. While building the baseline counter requires N F/Fs, the 2m F/Fs required to create the straight ring counter often outweigh them, regardless of how tiny the size mm of the low-order subcounter is. The pre-scaler authorized (PEN) signal, which generates ðNmÐ bits, is causing a substantial fan-out, which is causing the pre-scaled counter to run slower than expected. Paying attention to the fan-out issue is essential.

PROPOSED COUNTER

Before delving into the specifics of the high-speed counter's construction, this section provides a brief overview using novel state detection in the suggested LFSR counters.

State Extension and the LFSR:

Considering the FutureFor a visual representation of the intended LFSR timing with state extension, refer to Figure 5a. Both the LFSR stage cycles with and without the extension are shown in Figure 5b and 5c, respectively. Two holes, Q[1] and Q[2], are included into a 3-bit LFSR, called counter. demonstrates that this approach is successful with LFSRs of any size. Figure 5a shows that the suggested LFSR counter has a Galois, for instance, LFSR and a state monitoring circuit. The clock resets (nRST) signal coordinates the counter's activation, while the CNT signal initiates it. When considering the two possible outcomes, nRST = 0 or S[0] = 1.

It began at 11:12, and the status detection circuit beganat 02:00. Figure 5b shows that the standard 3 bits The states generated by LFSR range from 1112 to 1012, excluding occurrence 0002. To increase the total number of cycles to 2m, a specific technique isrequired, as an m-bit LFSR is limited to offering ð2m 1Ð. A solid circle in Figure 5c indicates that the status detection circuit has seen a trapezoidal shape bit pattern of 0012, the outcome of three successivecycles. At last, the first 02 element of the diagonal pattern is located using the state detecting circuit's F/F S[2]. Once that cycle ends, the 002 pattern is determined by the following F/F S [1] by

consultingS[2]'s 02 pattern. The initial F/F S[0] generates the 0012 design in the third cycle by using the 002 pattern found by S [1]. Figure 5c shows these detections as dotted lines. next the discovery of the 0012 vertical pattern, the next cycle will set S[0] to1 and reset the LFSR + state detecting circuit. Because of this, Q[2:0] = 1112 goes through two consecutive states. We can distinguish between the 0 and 7 states by comparing the parameters of S[0]. Byaltering the circuit bits and choosing the right starting value, we may construct an m-bit LFSR using this method and then identify a distinctive diagonal pattern that restarts the LFSR. The first m elements of an arrangement are linked to S[m1] at one place, and the value that is generated from Q[i] and S[i þ 1] is linked to S[i] at another place. By repeating this process m times, we may identify the diagonal pattern. A wide variety of low-order sub counters for the proposed LFSR counter are shown in Table 2. It is worth mentioning that several LFSRcounters yielded identical results.

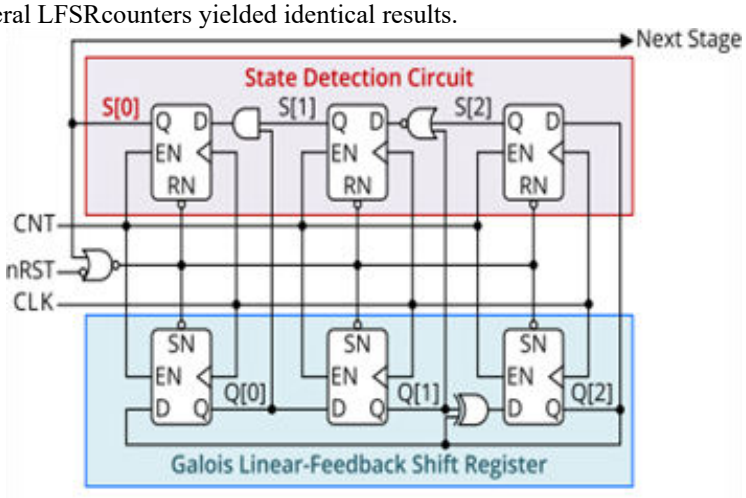

Fig: 3.1. State detection circuit

Additionally, by examining different basic polynomials, one might discover alternative detection patterns. The suggested state detection circuit is impacted by a gate delay and other components required to access F/Fs, which create a delay. This lag is similar to an LFSR with an XOR gate in the feedback route, sincethe circuit identifies a distinct horizontal pattern bit by bit. Due to its decreased latency, a simple fence is often used over an XOR gate in state detecting circuits. Therefore, the suggested LFSR counter's counting rate is comparable to the standard Galois LFSR. You can see the proposed one-stage LFSR brick counters and associated critical route diagramsin Figure 3. No matter the size of the LFSR, the feedback link is the most important path.

CLOCK GATING TECHNIQUE

Clock gating is a power-saving technique used by designers of advanced computer on a chip (ASIC) todisable clock signals to unused circuitry. Power intake, performance, and reliability may all be significantly improved by incorporating this criticalapproach within an ASIC design. The basic principle upon which clock gating is basedis simple. Gating circuits allow for the selective activation or deactivation of the clock signal for individual logic blocks or components. The gating circuit is controlled by a signal that indicates whether the element is in use or not. The gating circuit does not provide a clock signal to components that are not now active. By reducing thecircuitry's switching power usage, the ASIC's electrical usage is reduced. At many points in the design process, clock gating may be included into anASIC. You may implement clock gating logic at theRTL level by including it in the HDL code. Tools thatautomatically create gating hardware according to the timing constraints of the design allow clockgating to be done at the process of synthesis level. Itis possible to implement clock gating at the physicallayout level and then automatically insert gate cells into the netlist. Make sure the gating logic doesn't slow down the ASIC's critical pathway Unreported Phrase while employing clock gating. An ASIC's maximum working frequency is determined by the key path, it is the greatest route between its inputs and outputs. Thoroughly developing the gating logic will prevent the essential route from experiencing any more delays. It may be possible to do this by carefully placing the circuitry and determining the optimal locations for the gating cells. For the clock gate to function, the gating pulses mustbe perfectly synchronized with each other. This is caused by the fact that the various ASIC components depend on the clock signals to maintain functional synchronization. If the gating output and clock signal are not properly synchronized, data damage or loss might happen. To prevent this issue and maintain a synchronized gating signal, synchronizers, delay-locked loops (DLLs, or) are helpful tools.

Clock gating offers many potential benefits for ASIC designs. The most significant benefit is areduction in power use. By individually disabling clock signals to unused circuitry, the ASIC may become more power efficient without compromisingperformance. This is crucial since energy use is a bigfactor in devices that run on batteries. Gains in efficiency are only one of the many benefitsof clock gating. Reducing the switching behavior ofthe circuitry via the use of clock gating enhances theASIC's operating frequency while

decreasing the interconnect capacitor and inductance. Eliminating unnecessary nodes in the clock distribution chain isanother potential benefit of clock gating for ASIC performance and power usage. To further improve the ASIC's dependability, clock regulation is an additional option. Clock gating reduces switching action and heat load on the circuitry, which may increase the ASIC's longevity.Clock gating may help reduce the ASIC's electromagnetic field (EMI), which in turn makes itmore reliable.

Lastly, clock locking is a crucial technique for ASIC design that may reduce power consumption, increase reliability, and improve performance significantly. This method, which may be used at different points in the design process, requires careful preparation to prevent introducing additionaldelay in the ASIC's critical route. In order to meet the growing need for energy-efficient solutions, clock gating is increasingly being included into ASIC designs.

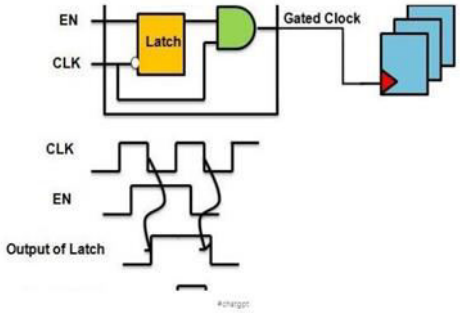

Fig 3.2. Clock diagram

4. Results:

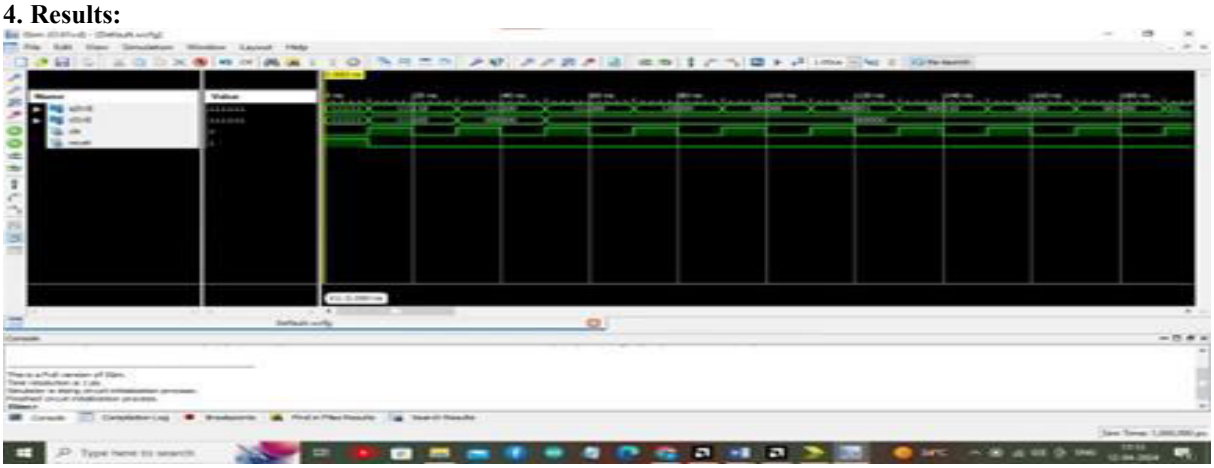

Fig:4.1. Simulation results

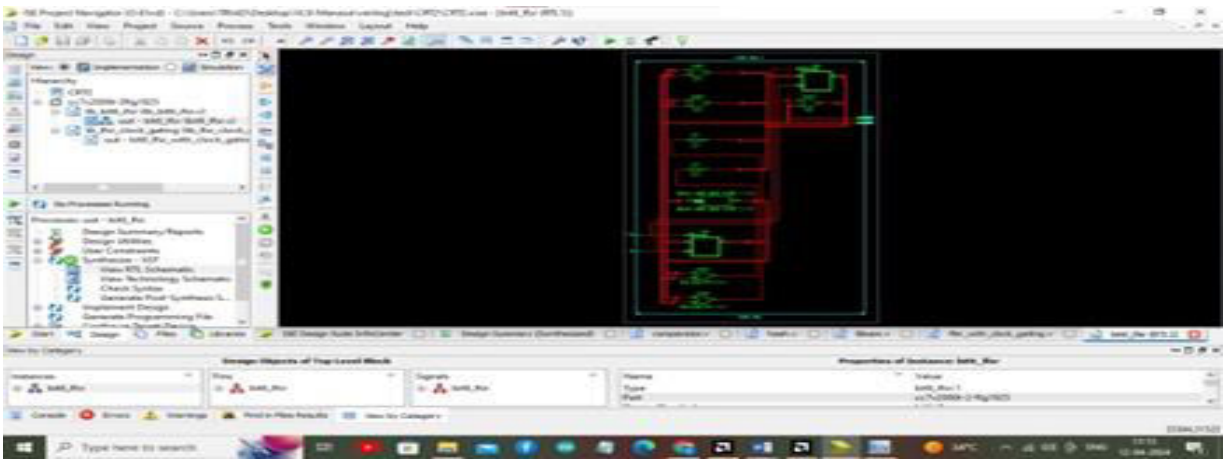

Fig:4.2. RTL view

4. CONCLUSION

Within the context of a high-speed counter design, this paper introduces a novel low-frequency-state-replication (LFSR) method. The identification of LFSR phases with reduced latency is possible because, by considering just one bit each time, an alternating Form cycles, an m-bit pattern was discovered. This distinctive diagonal pattern may bediscovered using m F/Fs plus m – 1Ð gates. The suggested counter uses a prescaled binary counter atthe top bit positions and is based on a small-scale LFSR clock. The upper half of the 64-bit counter is devoted to a conventional 58-bit binary counter,while the lower half is occupied by a 6-bit LFSR counter. Unlike the prior prescaled counter, which relied on a straight band counter to ensure accurate counting of each of the sub-counters, the new LFSR counter can detect a particular situation and maintain account of the high-order sub-counter. Using itsnovel state extension technique, the proposed m-bit LFSR counter achieves a counting rate that is nearlysize-independent and can traverse 2m states at the same pace as the conventional LFSR. The proposed 64-bit counter beats the multiple stages LFSR clock and the conventional binary counter at a speed of
2.08 GHz on 65 millimeter CMOS technology.

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